Status of the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. *(original)* A serial data interface system comprising:

a tone pattern generator configured to generate a tone pattern signal;

a selecting system configured to selectively pass the tone pattern signal or a data input signal;

a serializing device configured to serialize either the tone pattern signal or the data input signal;

a clock device configured to drive the tone pattern generator and the serializing device; and

a driver configured to differentially transmit the serialized tone pattern signal or the serialized data input signal.

2. *(original)* The system of claim 1, wherein the tone pattern signal comprises a continuous sequence of HIGH and LOW signals at a predetermined rate, such that the tone pattern signal represents a signal between approximately 49MHz and approximately 62MHz.

3. *(original)* The system of claim 1, wherein the tone pattern generator comprises:

a flip-flop.

4. *(original)* The system of claim 1, wherein the data input signal comprises a data signal and a driver control signal.

5. *(original)* The system of claim 1, wherein the tone pattern signal comprises a tone pattern portion and a driver control portion.

6. *(original)* The system of claim 1, further comprising one of a Beta port or a Bilingual port, wherein the tone pattern generator, the selecting device, the serializing device, the clock device, and the driver are positioned in the Beta port or the Bilingual port.

7. *(original)* The system of claim 1, wherein the serializing device also outputs a driver control signal.

8. *(original)* The Beta signal port of claim 7, wherein then driver control signal places the driver in active or inactive state.

9. *(original)* The Beta signal port of claim 1, wherein the selecting system comprises a multiplexer.

10. *(original)* The Beta signal port of claim 1, wherein the selecting system comprises a digital multiplexer.

11. *(original)* The Beta signal port of claim 1, wherein the clock device comprises a clock divider device that converts a high speed input clock signal to a low speed output clock signal.

12. *(original)* A system for determining data speed and connectivity between first and second Beta signal systems in serial data interface devices, comprising:

means for generating a tone pattern signal;

means for selecting the tone pattern signal or a data input signal;

means for serializing the tone pattern signal or the data input signal;

means for clocking the means for selecting and the means for serializing; and

means for transmitting one of the serialized tone pattern signal or the serialized data input signal to the second Beta signal system.

13. *(original)* The system of claim 12, wherein the means for generating a tone pattern signal comprises a flip-flop.

14. *(original)* The system of claim 12, wherein the means for selecting comprises a multiplexer.

15. *(original)* The system of claim 12, wherein the means for selecting comprises a digital multiplexer.

16. *(original)* The system of claim 12, wherein the means for transmitting comprises a driver.

17. *(original)* The system of claim 12, wherein the means for transmitting is placed into a first or second state based on the serialized signal.

18. *(original)* The system of claim 17, wherein the first state is a high impedance state and the second state is an active state.